AMENDMENTS

In the Claims:

Please amend the claims as indicated hereafter.

1. (Previously Presented) A processor purging system, comprising:

a translation lookaside buffer (TLB) having a plurality of translation pairs;

at least one memory cache; and

logic configured to make a determination whether at least one of the translation pairs corresponds to a purge signal and to purge, in response to the purge signal, each of the translation pairs in the TLB corresponding to the purge signal, the logic further configured to transmit, based on the determination, a purge detection signal indicative of whether at least one translation pair in the TLB corresponds to the purge signal and to determine, based upon the purge detection signal, whether to search the memory cache for information to be purged based on the purge signal.

2. (Canceled)

3. (Currently Amended) The system of claim [[2]] 1, wherein the memory cache further comprises an instruction queue.

4. (Original) The system of claim 3, wherein the memory cache further comprises a mini-TLB.

5. (Currently Amended) The system of claim [[2]] 1, further wherein the logic is configured to compare the purge signal with each of the plurality of translation pairs and to transmit a plurality of match signals corresponding respectively to the plurality of translation pairs, each of the match signals indicating whether the corresponding translation pair corresponds to the purge signal.

6. (Previously Presented) The system of claim 5, wherein the logic is further configured to collapse the match signals into the purge detection signal.

7. (Previously Presented) The system of claim 6, wherein the logic comprises a plurality of tiered logical AND gates configured to collapse the match signals into the purge detection signal.

8. (Previously Presented) The system of claim 6, wherein the logic comprises a plurality of tiered logical OR gates configured to collapse the match signals into the purge detection signal.

9-11. (Canceled)

12. (Previously Presented) A method for purging a processor, comprising the steps of:

detecting whether at least one of a plurality of translation pairs in a translation lookaside buffer (TLB) corresponds to a purge signal;

if at least one of the translation pairs in the TLB corresponds to the purge signal, purging the at least one translation pair corresponding to the purge signal;

transmitting, based on the detecting step, a purge detection signal indicative of whether [[a]] at least one of the translation pairs in the TLB corresponds to the purge signal; and

determining whether to purge an instruction queue based on the purge detection signal.

13. (Previously Presented) The method of claim 12, wherein the detecting step further comprises the steps of:

comparing the purge signal with each of the translation pairs; and

transmitting match signals, each of the match signals indicative of whether [[the]] a respective one of the translation pairs corresponds to the purge signal.

14. (Previously Presented) The method of claim 13, further comprising the step of collapsing each of the match signals into the purge detection signal.

15. (Canceled)

16. (Previously Presented) The method of claim 12, further comprising the step of purging, based on the determining step, the instruction queue if the purge detection signal indicates that at least one translation pair in the TLB corresponds to the purge signal.

17. (Previously Presented) A processor purging method, comprising:

detecting whether at least one translation pair in a plurality of translation pairs within a translation lookaside buffer (TLB) corresponds to a purge signal;

transmitting, based on the detecting step, a purge detection signal indicative of whether at least one of the translation pairs corresponds to the purge signal;

determining, based upon the purge detection signal, whether to search the memory cache for information to be purged based on the purge signal; and

if at least one of the translation pairs in the TLB corresponds to the purge signal, purging from the TLB the at least one translation pair corresponding to the purge signal.

18-20. (Canceled)

21. (Previously Presented) The system of claim 3, wherein the logic is further configured to determine whether to purge the instruction queue based on the purge detection signal.

22. (Currently Amended) The method of claim 12, further comprising the step of purging the instruction queue if the purge detection signal indicates that at least one of the translation pairs in the TLB corresponds to the purge signal.

23. (Previously Presented) The method of claim 12, wherein the determining step comprises the step of determining not to purge the instruction queue in response to the purge signal if none of the translation pairs correspond to the purge signal.

24. (Previously Presented) The method of claim 17, further comprising the step of purging an instruction queue in response to the purge signal if a detection is made in the detecting step that at least one of the translation pairs within the TLB corresponds to the purge signal.

25. (Previously Presented) A processor, comprising:

an execution unit;

an instruction queue coupled to the execution unit;

a translation lookaside buffer (TLB) configured to store a plurality of translation pairs, each translation pair having a respective virtual address and a respective physical address; and

logic configured to receive a purge signal and to make a determination as to whether any of the translation pairs stored in the TLB correspond to the purge signal, the logic configured to purge from the TLB each translation pair corresponding to the purge signal, the logic further configured to determine, based on the determination, whether to purge the instruction queue in response to the purge signal.

26. (Previously Presented) The processor of claim 25, wherein the logic is configured to purge the instruction queue in response to the purge signal if any of the translation pairs stored in the TLB correspond to the purge signal.

27. (Currently Amended) The processor of claim 26, wherein the logic is configured to refrain from purging the instruction queue in response to the purge signal [[if]] unless at least one of the translation pairs stored in the TLB corresponds to the purge signal.

28. (Previously Presented) A method, comprising the steps of:

storing a plurality of translation pairs in a translation lookaside buffer (TLB), each of the translation pairs having a respective virtual address and a respective physical address;

receiving a purge signal identifying at least one stale translation pair;

determining whether any of the plurality of translation pairs in the TLB are identified by the purge signal;

if at least one of the plurality of translation pairs in the TLB is identified by the purge signal, purging the at least one translation pair identified by the purge signal; and

determining whether to purge at least one component of a memory cache other than the TLB based on the step of determining whether any of the plurality of translation pairs in the TLB are identified by the purge signal.

29. (Previously Presented) The method of claim 28, wherein the step of determining whether to purge the at least one component step comprises the step of determining not to purge the at least one component if none of the translation pairs in the TLB is identified by the purge signal.

30. (Currently Amended) The method of claim 28, further comprising the step of, if at least one of the plurality of translation pairs in the TLB is identified by the purge signal, purging the at least one component in response to the step of determining whether to purge the ~~instruction queue~~ at least one component.

31. (Previously Presented) The method of claim 30, wherein the at least one component comprises an instruction queue.